REMARKS

Claims 1-30 are pending in this application. Claims 12-17, 29, and 30 are rejected. Claims 1-11 and 18-28 are herein canceled without prejudice in response to a restriction requirement. Claims 13, 29, and 30 have been canceled without prejudice and Claim 31 has been added herein.

Rejection Under 35 U.S.C. §112

Claims 12-17, 29, and 30 were rejected under 35 U.S.C.§112, first paragraph, as containing subject matter which was not described in the specification. Claims 13, 29, and 30 have been canceled.

Claim 12 has been amended to replace "first... device" with "buried vertical thyristor" and "second device" with "horizontally stacked pseudo-TFT transfer gate", as suggested by Examiner.

Claim 17 has been amended to recite "wordlines" rather than "wirings", as suggested by the Examiner.

The subject matter of amended Claim 12 is disclosed on page 4, lines 19-21, page 5, lines 4-16, and Figure 13 of the present Application. The subject matter of amended Claim 17 is disclosed on page 7, line 12 to page 8, line 10 of the present Application. Therefore, the rejection of Claims 12 and 17 under 35 U.S.C. §112, first paragraph should be withdrawn. Further, without conceding patentability per se of dependent Claims 14-17, it is respectfully submitted that the rejection under 35 U.S.C. §112 of Claims 14-17 should be withdrawn by virtue of their dependence on Claim 12.

Rejection of Claims Under 35 U.S.C. § 103(a)

Claims 12-17, 29, and 30 were rejected under 35 U.S.C.§103(a) as unpatentable over U.S. Patent No. 6,448,586 (Nemati) in view of U.S. Patent No. 5,357,125 (Kumagi).

Nemati and Kumagi, either separately or in combination, do not disclose a horizontally stacked pseudo-TFT transfer gate recited in Claim 12 as amended. The Examiner states that Nemati discloses this element. See Nemati, at column 7, lines 1-15 and Figure 8, which reads:

> ...stripes or different combinations of cells and/or stripes in the top view layout. Each of the plurality of PNPN-type NDR devices is constructed in a manner similar to the structure of FIG. 1, however, with respective control ports being provided by interconnected charge plates (or gates) 48 primarily adjacent to the upper N region of each PNPN-type NDR device. The power thyristor quickly changes between a current-passing mode and a current-blocking mode in response to an activation signal presented to the interconnected charge plates 48. This approach is advantageous since a quick state change is realized using a relatively low voltage. Moreover, this form of power thyristor can be readily expanded in terms of the number of NDR devices for high power applications or reduced in number for lower power applications.

All gates in Nemati, and particularly the gates 48 referred to by Examiner, have their source/drain and body on a substrate – note that the gates 48 are on a p-layer which is disclosed by Nemati to be a substrate (see Nemati Figures 1, 6, 7, and 8). In contrast, it is inherent in a pseudo-TFT gate as recited in Claim 12 as amended that both the source/drain and the body are contained in a polysilicon layer. Therefore, it would not be obvious for someone skilled in the art to use pseudo-TFT gates instead of the gates 48 disclosed by Nemati, because gates on polysilicon have different electron mobility characteristics from gates on a silicon substrate.

Further, Nemati teaches away from the invention, because Nemati requires a metalization layer 19 or 42 as an anode on the surface of the thyristor, which is where the horizontally stacked pseudo-TFT transfer gate of Claim 12, as amended, is located (see Nemati column 4, lines 18-21, column 6, lines 62-64, and Figures 1, 6, 7, and 8).

The Examiner cites Kumagi as disclosing a thyristor buried underneath a gate which

covers the entire top surface of the thyristor, the gate forming a planar top surface of the T-RAM cell. See Kumagi, at column 5, lines 61-68 and Figures 1-5, which reads:

> [Here, the gate] electrodes are disposed on the surface between the n+ regions 56 and the n+ region 64 via a gate insulating film 57. A source electrode 21, which makes contact not only with the p+ contact regions 68 formed on the p regions 67, but also with the source regions 56 of the MOSFET 2, shortcircuits the source regions 56 to the gate region 67 of the SI thyristor, resulting in the equivalent circuit shown in FIG. 3.

The elements for which Kumagi is cited do not cure the defects of Nemati as described above, and in particular, Kumagi does not disclose a horizontally stacked pseudo-TFT transfer gate recited in Claim 12 as amended.

Thus, Nemati and Kumagi, either separately or in combination, neither teach nor suggest the recitation of Claim 12 as amended. Therefore, Claim 12 is believed to be allowable over Nemati in view of Kumagi.

Without conceding patentability per se of dependent Claims 14-17, it is respectfully submitted that Claims 14-17 are believed to be allowable over Nemati in view of Kumagi by virtue of their dependence on independent Claim 12 as amended.

Moreover, Nemati does not disclose wordlines fabricated on a planar top surface as recited in amended Claim 17. Instead, Nemati only discloses word lines fabricated alongside a thyristor, rather than on a planar top surface. See Nemati, at column 4, lines 19-21 and Figures 1 and 6-8, which reads: "At the top of the vertical NDR device 10 is a metalization layer 19 that is used for connecting the top terminal of the device to a supply or reference voltage, Vref." Thus, the device disclosed by Nemati is unsuited to the fabrication of wordlines on the top surface, because the top surface of the transistor disclosed by Nemati is covered by a metalization layer 19 or 42 serving as an anode carrying Vref, and contact between wordlines and Vref would presumably interfere with wordline operation (see Nemati, Figures 1 and 8). Kumagi does not

disclose wordlines, therefore Nemati cannot be combined with Kumagi to produce the device claimed in amended Claim 17.

New independent Claim 31 was added to more completely claim elements of the present invention. Specifically, Claim 31 recites a transfer gate which covers "a part of a top surface of said thyristor". The subject matter of Claim 31 is disclosed on page 4, lines 19-21, page 5, lines 4-16, and Figure 13 of the present Application. Kumagi discloses a gate covering the entirety of a top surface of a thyristor. Nemati does not disclose a gate covering any portion of a top surface of a thyristor. Thus, Nemati and Kumagi, either separately or in combination, do not disclose a transfer gate covering a part of a top surface of a thyristor as recited in new Claim 31. Therefore, Claim 31 is believed to be allowable for at least these reasons, as well as the reasons given above with respect to Claim 12.

Applicants submit that pending Claims 12, 14-17, and 31 are now believed to be in condition for allowance. Allowance is respectfully requested. Should the Examiner believe that a telephone conference or personal interview would facilitate resolution of any remaining matters, the Examiner may contact Applicants' attorney at the number given below.

Respectfully submitted,

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